

Innopower miniIP+™ Platform

High-Density Library and Small Area I/O IP in 0.13µm, 0.11µm, 65nm and 55nm Technologies

Overview

Cost and power consumption are two dominant issues for chips selling into consumer or portable device markets. Innopower's miniIP+™ platform is a complete IP portfolio optimized for chip designers to reduce die size and power dissipation. It promises customers considerable cost advantages and much longer product battery life, two of the most important features consumers care about.

Innopower's miniIP+™ portfolio is a collection of full-function essential IPs with drastically reduced area and power consumption.

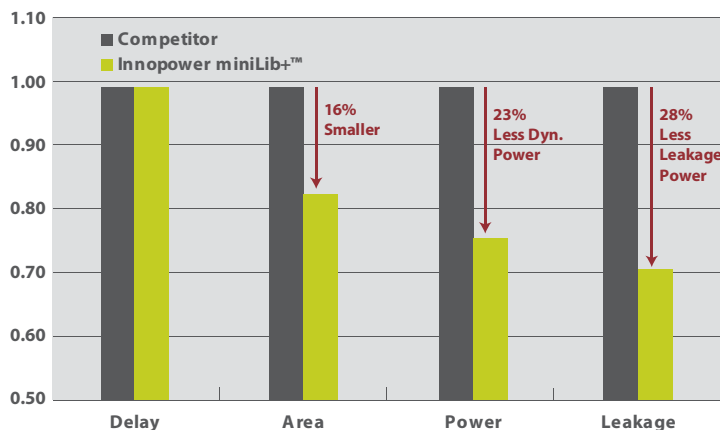
miniLib+™

miniLib+™ comes with 16% reduction in core logic area, compared with the other high density cell libraries. Its dynamic power and static power can be reduced by 23% and 28% respectively.

Features

- Optimized for high-density & low-power applications
- Area features:
 - Best cell architecture of ultra high density in industry
 - Rich set of cell functions for logic optimization
- Low power features
 - Circuit design aiming at minimized dynamic and leakage power
 - Low-drive cells available for power optimization
- Performance features
 - Powerful driving strength for timing closure
 - Fast circuit structure for arithmetic cells (adder, XOR, and etc.)

Comparison



- Condition: Typical Case (TT, 1.2V, 25°C)
- The benchmark is obtained from the results after synthesis and is averaged over 21 test cases, including CPU, DSP, protocol IP, control and interface logic, and etc.
- The competitor uses PWL waveforms for timing characterization, resulting in overly optimistic timing performance at the expense of sacrificial design margin.

Target Applications

- Portable multimedia player
- Home networking
- Digital camera
- Cell phone
- Thumb drive
- GPS
- PDA



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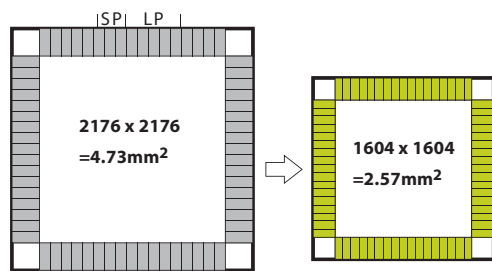
Characteristic	Innopower's miniLib+™	Competitor's high density Library
Process	0.13µm Logic	0.13µm Logic
Device	SVT	SVT
Gate density (gate/mm ²)	330K	283K
Core cell height (Grid) X/Y	6 tracks, 2.46µm	7 tracks, 2.87µm
Routing grid (µm) P	0.41/ 0.41	0.41 / 0.41
Routing direction	HVHV	HVHV
Metal usage	Metal1	Metal1
Cell number	609	618
Function number	119	130

miniIO+™

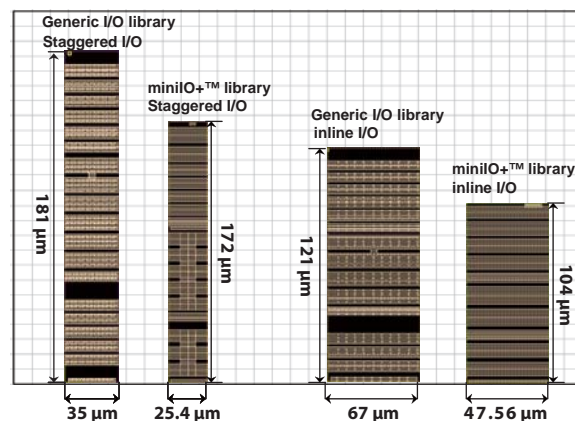
miniIO+™ is a small area I/O with robust ESD protection. Compared with general I/O pads, it comes with about 30% area reduction while achieving better ESD performance.

Features

- About 30% area reduction while achieving better ESD performance
- Offer same programming I/O's functionality (PIOS) as generic I/O library
 - Input PU/PD resistor, keeper, Schmitt-trigger
 - Output programmable drive strength from 2mA to 16mA
 - Support multiple voltages 3.3V/2.5V/1.8V
- Built-in antenna diodes for all pins
- Low input/output capacitance to help reduce I/O power consumption



For a pad-limit design with 200 pin count 45% area is saved with miniIO+™



Availability

Innopower's miniLib+™ and miniIO+™ are now available in 0.13µm, 0.11µm, 65nm and 55nm processes. The miniLib+™ and miniIO+™ have been silicon proven in various foundries through real chips.



INNOPOWER TECHNOLOGY CORPORATION
www.innopower-tech.com

HEADQUARTERS, TAIWAN
> Hsinchu, Taiwan > Tel: 886.3.563.5228 > IP_sales@innopower-tech.com